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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/075,539	02/14/2002	Gunnar Krause	P2001,0099	8630

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EXAMINER

WANG, ALBERT C

ART UNIT	PAPER NUMBER
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2115

DATE MAILED: 02/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/075,539

Applicant(s)

KRAUSE ET AL.

Examiner

Albert Wang

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-11 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 02/14/02.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_.

### **DETAILED ACTION**

1. Original claims 1-11 are pending.

#### ***Claim Objections***

2. Claim 2 objected to because of the following informalities: "and," is interpreted as "and". Appropriate correction is required.

#### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 5 and 11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 5 recites the limitation "said command decoder". There is insufficient antecedent basis for this limitation in the claim. Claim 11 depends on claim 5.

#### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1, 9, and 10 are rejected under 35 U.S.C. 103(a) as being obvious over Wu et al, U.S. Patent No. 6,507,888 ("Wu"), in view of Kim et al., U.S. Patent No. 6,134,180 ("Kim").

As per claim 1, Wu teaches a memory configuration, comprising:

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at least two semiconductor memory modules, including a first semiconductor memory module and a second semiconductor memory module (fig. 2, SDR module arrays 230 and 240), controlled by internal clock signals (fig. 1, clock signal MCK; col. 3, lines 57-61; fig. 2, conversion device 220 signals to both SDR module arrays), said two semiconductor memory modules output or receive data in SDR mode;

an interface device for receiving or outputting the data in DDR mode (fig. 2, chipset 210; col. 3, lines 41-52, chipset 210 supports DDR); and

a conversion device connected between said interface device and said two semiconductor memory modules to route the data for outputting or reception (fig. 1, conversion device 10; fig. 2, conversion device 220).

However, Wu does not expressly teach SDR mode as outputting or receiving data only on one of a rising edge and a falling edge of a clock signal. Kim teaches that SDR mode allows reading or writing a single word on every rising (or falling) edge of a clock signal (col. 1, lines 19-29). At the time of the invention, it would have been obvious to one of ordinary skill in the art Wu's semiconductor memory modules implicitly output or receive data only on one of a rising edge and a falling edge of a clock signal, since such implementation of single data rate (SDR) mode is well established (Kim, col. 1, lines 19-29).

Kim teaches further that DDR mode allows receiving data on a rising edge and a directly succeeding falling edge of an external clock signal (figs. 2 & 5, write data W0a and W0b are center aligned with rising and falling edges of external clock; col. 1, lines 56-67), and allows outputting data between the rising edge and the directly succeeding falling edge of the external

clock signal (figs. 2 & 5, read data R2d and R2b are edge aligned with rising and falling edges of external clock).

As per claim 9, Wu teaches said conversion device contains a signal generator for generating a clock signal (fig. 1, clock controller 120; col. 3, lines 57-61). Kim teaches the edges of a clock signal are oriented to edges of a data signal during a data outputting (fig. 5, edges of strobe oriented to read data R3d; col. 8, line 66 – col. 9, line 5; col. 9, lines 49-59) and are oriented to a binary signal level of the data signal during a data inputting (fig. 5, edges of strobe oriented to write data W0a, W0b; col. 5, SDR mode is similar).

As per claim 10, Wu teaches said conversion device has at least two further memory modules for storing a respective further bit of a data word, one of said further memory modules is connected in parallel with said first semiconductor memory module and another of said further memory modules is connected in parallel with said second semiconductor memory module (fig. 5, conversion device 520 has modules 540-546 connected in parallel).

5. Claims 2-4, and 6-8 are rejected under 35 U.S.C. 103(a) as being obvious over Wu/Kim, as applied to claims 1 and 2 above, and further in view of Karabatsos, U.S. Patent No. 6,2446,158.

As per claim 2, Kim teaches feeding the external clock signal to an interface device (fig. 3, external clock K; col. 5, lines 29-32), and generating complementary clock signals (fig. 3, complementary strobe KQ; col. 8, line 66 – col. 9, line 5). However, Kim does not expressly teach separately feeding individual complementary clock signals to first and second memory modules. Karabatsos teaches feeding a first clock signal to a first memory module, and feeding a

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delayed version of the first clock signal to a second memory module (fig. 3A, 100 MHz to memory chip A and delayed 100 MHz to memory chip B). Karabatsos further teaches that the delayed clock signal is a complementary signal (figs. 3C & 3E; col. 5, lines 49-54, delayed by on half period). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Karabatsos' separate feeding of individual complementary clock signals to Wu/Kim's memory configuration. A motivation for doing so would have been to facilitate DDR operation with SDR memory modules (Karabatsos, col. 6, lines 23-33).

As per claim 3, Karabatsos teaches generating complementary clock signals with a phase locked loop (fig. 6; col. 9, lines 3-14). A delay locked loop is a variation of a phase locked loop.

As per claim 4, Wu teaches said conversion device has a command decoder for detecting a command for receiving data (fig. 1, instruction controller 122). Kim teaches a command decoder (fig. 3, control logic 304) for which the command for receiving data contains at least two signal pulses present on the rising edge of the external clock signal (fig. 5, signals B1-B3; col. 6, lines 12-22 & 34-42). Karabatsos teaches a half clock period delay between first and second memory modules (fig. 3A; col. 5, lines 49-54).

As per claim 6, Kim teaches the command for receiving data contains the two signal pulses that each have a low level and are centered with respect to two rising edges of the external clock signal that are separated by two clock periods (fig. 5, signals B1 and B3 are separated during periods C2 and C3).

As per claim 7, Karabatsos teaches individual switches for each memory module (fig. 3A, switch 110 for chip A and switch 111 for chip B), which are dependent on the external clock

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signal (figs. 3D & 3F). A three terminal, changeover switch would be an obvious substitute for the two individual switches.

As per claim 8, Karabatsos teaches alternately connecting the data bus between the two memory modules (col. 6, lines 2-21).


### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert Wang whose telephone number is 571-272-3669. The examiner can normally be reached on M-F (9:30 - 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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January 26, 2005

  
THOMAS LEE  
PATENT EXAMINER  
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